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Design and Implementation of 64-Bit Ripple Carry Adder and Ripple Borrow Subtractor Using Reversible Logic Gates

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ABSTRACT

Minimal power design is desirable for a range of applications, including the Internet of Things (IoT), quantum computing, and so on. The reversible logic approach is at the foundation of a new technique for designing minimal power digital logic circuits for quantum computing applications. The reversible logic circuit offers a whole new approach to quantum computer processing. Reversible logic gates-based devices will be in high demand for future computer technologies since they require less power. Reversible logic gates were used to design a ripple carry adder (RCA) and a ripple borrow subtractor (RBS), which were simulated in Verilog 2018.3 and coded in Verilog HDL.

Keywords - **Constant Inputs, Garbage Outputs, Reversible Logic, Quantum Cost, Ripple Carry Adder (RCA), Ripple Borrow Subtractor (RBS).**

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I. INTRODUCTION

The Full Adder (FA) is a logical arithmetic computational circuit that calculates the sum of 3 single bits together. It contains three inputs: a, b, and cin, as well as two outputs: s and cout, with cin denoting Carry-In and cout denoting Carry-out respectively. A full subtractor (FS) that implements a combinational logic circuit. It has three inputs a, b, bin, and two outputs d, the bout with bin signifying Borrow-In and bout indicating Borrow-Out, respectively.

To add an N-bit number, multiple FA circuits can be cascaded in parallel. In an N-bit parallel adder, there must be N FA circuits [1-3]. The carry-out of each full adder is fed to the carry-in of the next most significant FA in an RCA. It's considered an RCA since each carry bit ripples into the subsequent steps. The s and cout bits of any half adder stage in an RCA is not valid until that stage's carry-in executes. This is caused by propagation delays within the logic circuitry [4-5].

Subtracting circuits produce an N-bit output and a borrow-out bit by combining two N-bit operands. The full subtractor can be utilized to create an RBS that can subtract any two N-bit values; however, RBS circuits are as slower as RCA circuits. The approach is similar to that of designing an adder, in which the circuit is constructed from the truth table. Energy is discharged into the environment by the irreversible logic gate. To put it another way, information loss equates to energy loss. When a computer executes a logic operation, it erases data. Current irreversible logic methods generate a lot of heat, which shortens the circuit's lifespan.

The reversible circuits are theoretically demonstrated for offering nearly energy-free computation by preventing information loss during operations. Hence, reversible logic will meet the requirements of power, speed, and size in the EDA (Electronic Design Automation) industry.

II. REVERSIBLE LOGIC

2.1. Basic Terminologies

The following are the main terms used in reversible logic computations [6-8]:

(i)Quantum Cost: It equals the overall cost of the circuit's basic gates. It is the cost of implementing the reversible circuit using the NOT and CNOT gates. Basically, the cost of the design in the specifications of a fundamental gate's part is assigned to it.

(ii) Constant Inputs: Constant inputs are pairs of inputs that are fixed at a constant value of either logic '0' or '1' in order to generate the specified logical function.

(iii) Garbage Outputs: Garbage output refers to the output that is neither an output utilized for further computations nor an input to another gate. Constant input + Input = Garbage output + Output

(iv) Reversible Logic: A digital circuit with k outputs if there are k inputs. Each combination in the output is distinct from the input. This is referred to as one-on-one correspondence and is depicted as k*k.

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2.2. Basic Reversible Logic Gates

The basic reversible logic gates are Feynman, Toffoli, Peres, and Fredkin gates [9-11].

(i)Feynman Gate: The Feynman Gate is a 2x2 reversible logic gate. Quantum cost = 1. Fig1 depicts the Feynman gate.

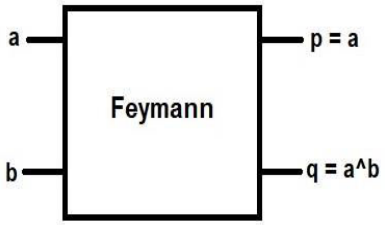

Figure 1. Feynman gate

(ii) Toffoli Gate: The Toffoli gate is a 3*3 gate. Quantum cost = 5. The Toffoli gate is depicted in Fig 2.

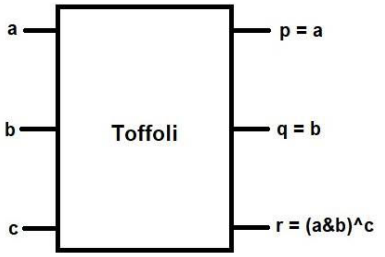

Figure 2. Toffoli gate

(iii) Fredkin Gate: The Fredkin gate is a 3*3 gate. Quantum cost=5. The Fredkin gate is shown in Fig 3.

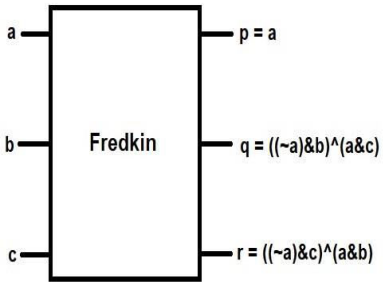

Figure 3. Fredkin gate

(iv) Peres gate: The Peres gate is a 3*3 gate. Quantum cost = 4. The Peres gate is depicted in Fig 4.

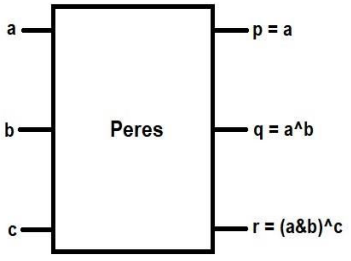

Figure 4. Peres gate

III. PROPOSED REVERSIBLE ADDER AND SUBTRACTOR

A reversible RCA and a reversible ripple borrow subtractor has been designed using DKG gates. When a=0, the DKG gate can function as a FA, and when a=1, it can function as an FS, with the input bit acting as a control bit.

3.1 DKG gate

Figure 5 depicts a 4*4 reversible logic-based DKG gate that can be used as a reversible FA or FS. It is possible to verify that the input combination that corresponds to a certain output combination may be identified in a distinctive manner. If input a=0, the DKG gate acts as a reversible FA, and if input a=1, it acts as a reversible FS. The quantum cost is six.

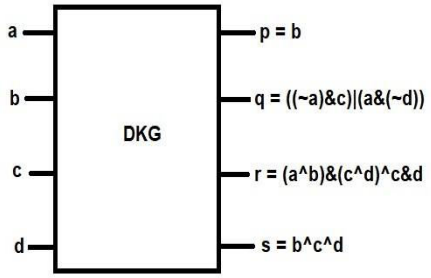

Figure 5. DKG gate

3.2 Reversible Ripple Carry Adder

The FA is the most fundamental element of an RCA. By cascading the FAs in a predetermined sequence, the DKG gate is utilized to produce a reversible RCA. The output equations of an RCA are represented as in equations 1 & 2:

$$Si = Ai \hat{} Bi \hat{} Ci \quad (1)$$

$$Ci+1 = (Ai \hat{} Bi)\ \&\ Ci\ \hat{}\ AiBi \quad (2)$$

where i=0, 1, 2….

By setting a=0, the DKG gate is used. As a result, the DKG gate functions as a FA. To make a ripple carry adder, these adders are cascaded in a predetermined sequence.

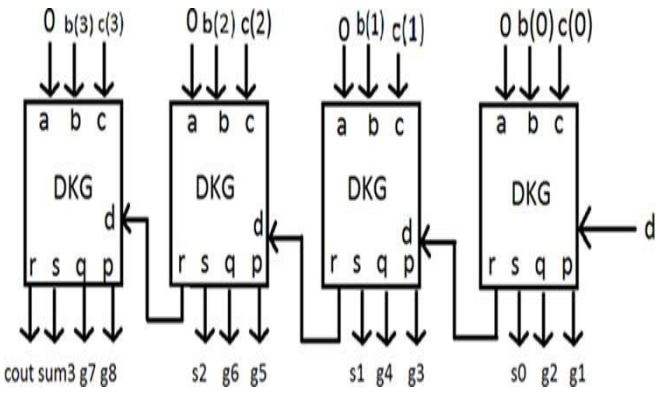

Figure 6. 4-bit RCA using DKG gate

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Figure 6 illustrates a DKG gate-based 4-bit ripple carry adder design. There are four constant inputs, eight garbage outputs, 24 quantum costs, and four reversible logic gates in this design. The design is also extended to 16-bit and 64-bit, as shown in figures 7 and 8, respectively.

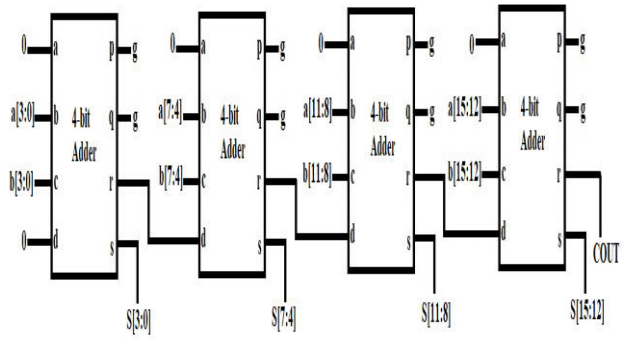

Figure 7. 16-bit RCA using DKG gate

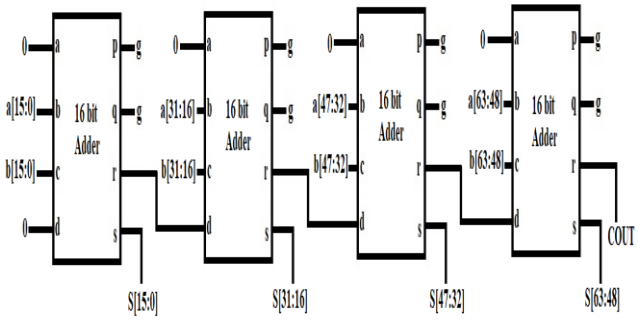

Figure 8. 64-bit RCA using DKG gate

3.3 Ripple Borrow Subtractor

Using a 1-bit reversible FS, the N-bit reversible subtractor can be generated by cascading a reversible FS using the concept of ripple borrow design. A reversible N-bit subtractor subtracts the N-bit values Ai and Bi, where $0 \leq i \leq n-1$. A ripple borrow subtractor's basic building component is the full subtractor. The DKG gate is used to create a reversible ripple borrow subtractor, which is obtained by cascading the full subtractors in sequence. A ripple borrow subtractor's output expressions are given by equations 3 & 4:

$$Di = Ai \wedge Bi \wedge Bin \quad (3)$$

$$Bi+1 = \sim(\sim Ai \wedge Bi) \,\&\, Bin \wedge AiBi \quad (4)$$

where i=0, 1, 2….

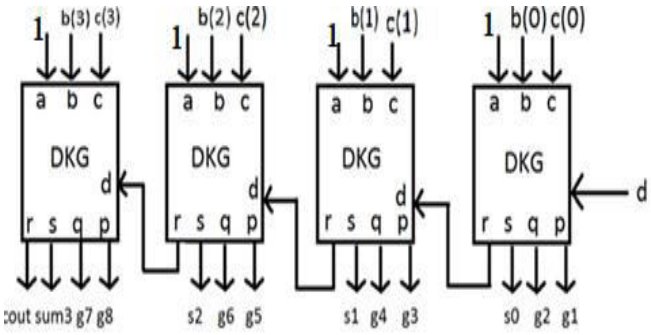

Figure 9. 4-bit RBS using DKG gate

Here is DKG gate is used by making A=1. Hence the DKG gate acts as a full subtractor. TFigure9 depicts the 4-bit ripple borrow subtractor using the DKG gate. Similarly, the design is extended to 16-bit and 64-bit as depicted in Figures 10 and 11 respectively.

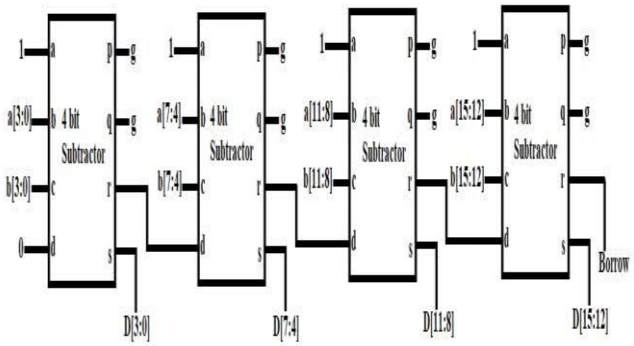

Figure 10. 16-bit RBS using DKG gate

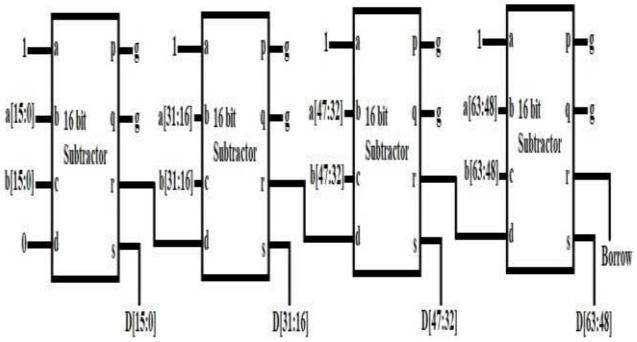

Figure 11. 64-bit RBS using DKG gate

IV. RESULTS AND OBSERVATIONS

A ripple carry adder and a ripple borrow subtractor has been designed using reversible logic DKG gate. The design was first designed for 4-bit and then later extended to 16-bit and 64-bit. The results were simulated in Xilinx Vivado 2018.3 and the coding style used was Verilog HDL.

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Reversible logic computations are one of the most promising strategies for lowering power consumption, as these circuits are theoretically capable of providing nearly energy-free computation systems while retaining information loss. The properties of reversible logic gates were analyzed, as well as some of their illustrative implementations [1]. The varieties of logic gates, various uses, and how they can be implemented on these logic gates are explained in this work. The adder-subtractor circuit and its implementations are included in this paper [3].

The optimal approach for developing reversible ripple-carry adders is the focus of this work. According to Landauer's [5] principle, the designs suggest that the amount of output information is equal to the amount of input information, implying that they can (at least potentially) function with arbitrarily low dissipation [4].

4.1 Simulation result

The simulations are obtained for 64-bit RCA and 64-bit ripple borrow subtractors using Xilinx Vivado 2018.3. The waveforms for 64-bit RCA and 64-bit ripple borrow subtractor are shown in figure 12 and figure 13 respectively.

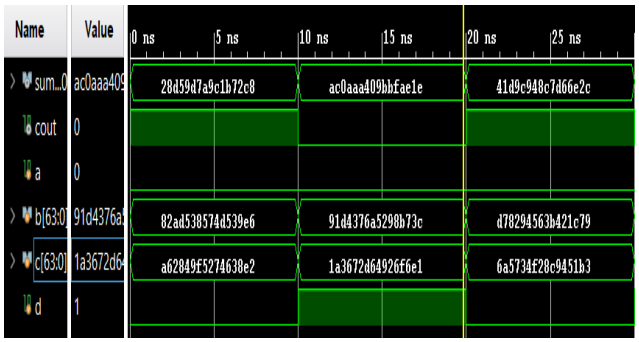

Figure 12. 64-bit RCA

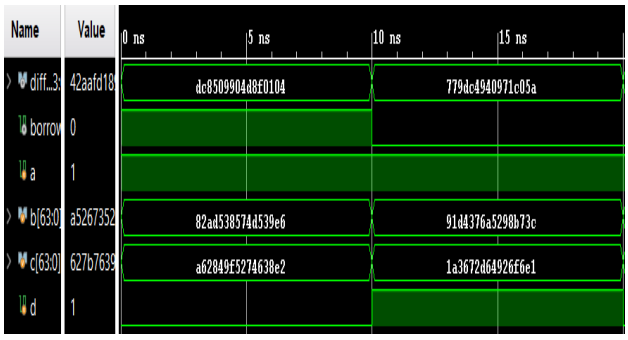

Figure 13. 64-bit RBS

4.2 Implementation & Design metrics

The Quantum cost, garbage output, constant input and amount of reversible gates of the RCA and ripple borrow subtractor designed for 4-bit are given in Table I.

Table 1. Design cost metrics for 4-bit RCA & RBS.

Design	Number Of Gates	Constant Inputs	Garbage Outputs	Quantum Cost
RCA	4	4	8	24
RBS	4	4	8	24

Functional verification of the 64-bit RRCA is done by the Xilinx Vivado tool. Figure 14 & figure 15 shows the RTL schematic for 16-bit & 64-bit RCA. The RCA employs DKG gate as one-bit full adders

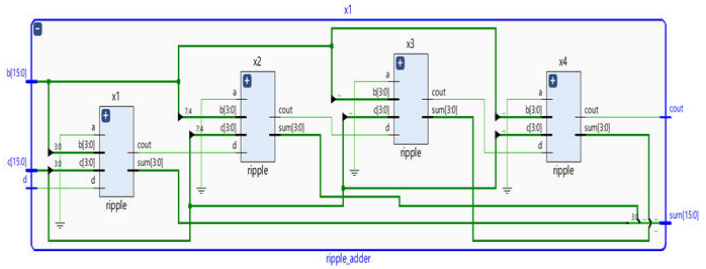

Figure 14. RTL schematic for 16-bit RCA

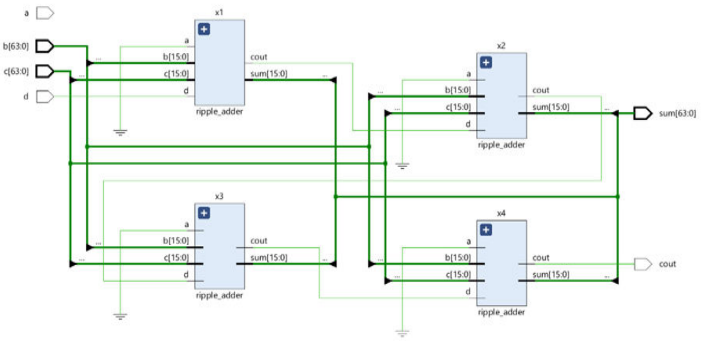

Figure 15. RTL schematic for 64-bit RCA

V. CONCLUSION

The key purpose of this study is to enhance a better understanding of reversible logic computations. The circuit consists of a single unit that, depending on the requirements and the control bit A selection, can serve as an adder or a subtractor. The amount of garbage output bits produced by reversible computation is kept to a minimum, and the value depends on the computation's input as well as reversible gates utilized and their co-relation. As a result, dissipation can be eliminated by making computations reversible. The use of such designs can be advantageous in order to maximize efficiency as well as minimize power consumption.

DNA computing, Quantum computing, Cryptography, Quantum Computing Automata, Nano computing, Communication, Optical computing, and other applications can all benefit from reversible logic circuits.

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